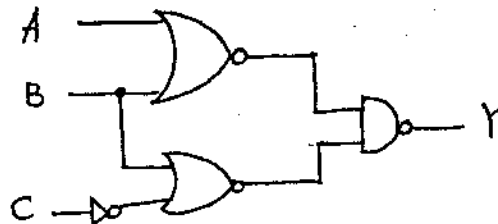


- N.B.** (1) Question No.1 is compulsory.
 (2) Attempt any **four** questions out of remaining **six** questions.
 (3) Assume **suitable** data if **required**.

1. (a) Convert the following binary numbers to Decimal, Hexadecimal and Octal forms :— **5**
 (i) $(101101.1101)_2$
 (ii) $(11011011.100101)_2$
 (b) State and explain De Morgan's Theorem. **5**
 (c) Determine the truth table for the circuit given — **5**



- (d) Implement the following Boolean function using 8 : 1 MUX :— **5**
 $F(P, Q, R, S) = \sum m(0, 1, 3, 4, 8, 9, 15)$
2. (a) Design a BCD to Seven Segment Display decoder. **10**
 (b) Convert :— **10**
 (i) JK F/F to D F/F (ii) T F/F to D F/F
3. (a) Simplify the following boolean function by using a Quine Mc Cluskey Method :— **10**
 $F(A, B, C, D) = \sum m(0, 2, 3, 6, 7, 8, 10, 12, 13)$
 (b) Design 2 bit comparator using gates. **10**
4. (a) Compare :— **10**
 (i) PLA and PAL
 (ii) Moore and Mealey Machine.
 (b) What is meant by Shift Register ? Give its applications. **10**
5. (a) The following pulse train is to be generated by a counter. Draw the logic diagram :— **10**
 Pulse train :— 10101.
 (b) Design a binary to BCD Converter. **10**
6. (a) The input to the combinational logic circuit is a 4 - bit binary number. Design the logic circuit with minimum hardware for following :— **10**
 (i) Output $Z_1 = 1$, if the input binary number is '5' or less than '5'
 (ii) Output $Z_2 = 1$, if the input binary number is '9' or more than '9'.
 (b) Explain Master-slave J-K Flip-Flop. **10**
7. Write short notes on any **two** of the following :— **20**
 (a) ALU (c) CAD Tools
 (b) FDGA (d) VHDL Features.