

Sem III [R.W] Comp / E.O.F.A / Dec. 09

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Con. 5702-09.

(REVISED COURSE)
(3 Hours)

SP-7362

[Total Marks : 100

- N.B. :** (1) Question No. 1 is **compulsory**.
(2) Solve any **four** questions out of **remaining**.
(3) Draw **neat** labelled diagram wherever **necessary**.

1. (a) Explain Vonnewmann model in detail. 5
(b) Define the following terms microinstruction, microoperation, microprogram. 5
(c) Explain with suitable example Booth's Algorithm for Signed Multiplication. 10
2. (a) Explain in detail characteristics of RISC and CISC. 10
(b) Explain restoring division method, Hence perform $17/3$. 10
3. (a) What is the difference between pipelining and parallelism ? Explain the Flynn's Classification in detail. 10
(b) Explain in brief about SPARC processor. Draw and explain in brief n-bit Windows architecture of SPARC processor. 10
4. (a) How many 128 bytes RAM chips are required to provide a memory of 2048 bytes ? Show details of connections, clearly indicating address, data and decoder configuration. 10
(b) Explain the different RAID levels. 10
5. (a) Explain page replacement algorithm. Find out page fault for following string using LRU method. 10
6 0 12 0 30 4 2 30 32 1 20 15
(Consider page frame size = 3).
(b) Explain the interleaved memory in detail. 10
6. (a) What is Cache coherence ? Explain Cache coherence strategies in single processor and multiprocessor systems. 10
(b) Write short notes on (any two) :- 10
 - (i) DMA
 - (ii) Programmed I/O
 - (iii) Interrupt Driven I/O.
7. (a) Explain systolic processor with suitable example. 10
(b) What is pipelining ? Explain six stage CPU instruction pipeline. 10