

- N.B. :** (1) Question No. 1 is compulsory.
 (2) Attempt any four questions out of remaining six questions.
 (3) Assume suitable data if required.

1. (a) Explain the following term in relation to PLL :- 5
 - (i) Lock range
 - (ii) Capture range.
- (b) Explain switch Debouncing with circuit diagram. 5
- (c) Explain following term with reference to DAC. 5
 - (i) Linearity
 - (ii) Resolution
 - (iii) Accuracy.
- (d) Compare active filter and passive filter. 5
2. (a) Obtain the transfer function for KRC low pass filter and draw the circuit. 10
 Calculate the component value if $f_0 = 2$ kHz. and $Q = 4$.
- (b) Explain VCO IC 566 and its features. 10
3. (a) Explain Monostable multivibrator using IC 555 with the internal circuit diagram 10
 of IC 555, draw the wave form. Calculate the value of R and C for pulse width of 20 ms.
- (b) What are the performance parameters of DAC. Explain any one technique 10
 of DAC.
4. (a) What is Instrumentation amplifier, explain it with three opamp, and write down 10
 advantages and disadvantages of it.
- (b) Explain opamp as voltage to current converter and mention the application 10
 of V-I converter.
5. (a) Design a Moore machine for overlap sequence detector for the string "1110". 10
 The output must be '1' when the input matches this string -
 - (i) Draw the state diagram
 - (ii) Write its transition and output table
 - (iii) Draw its Logic diagram.
- (b) Draw and explain the block diagram of FPGA. 10

6. (a) Write VHDL code for a four bit up counter. 8
(b) A fundamental-mode circuit is to have two inputs and a single output, which becomes '1' only upon the occurrence of the last in the following sequence of input combination, otherwise $z = 0$. 12

$x_1 x_2 : 00011110$
Construct primitive flow table.

7. Write short notes (any three) :-

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- (a) Structural Modelling
- (b) Races and Cycles
- (c) Compare Static and Dynamic RAM
- (d) Log Amplifier.

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DATE : 01/11/11

(REALISED COURSE)

3 Hours

VI SEM