

- N.B.** (1) Question No. 1 is compulsory.
 (2) Attempt any four questions out of remaining six questions.
 (3) Assume suitable data if necessary.

1. (a) Explain the difference between error detecting codes and error correcting codes. 5
 (b) Determine the value of x, 5
 $(211)_x = (152)_8$.
 (c) Explain D Flip-Flop. 5
 (d) 4-bits magnitude comparator. 5

2. (a) Explain interfacing of T.T.L. and CMOS logic families. 8
 (b) Explain parameter's of logic families. 8
 (c) Explain RTL logic family. 4

3. (a) Prove the following using Boolean Theorems :— 6
 (i)
$$\left[(C + \bar{C}D)(C + \bar{C}\bar{D}) \right] \left[(AB + \bar{A}\bar{B} + A \oplus B) \right] = C$$

 (ii)
$$\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC = AB + AC + BC$$

 (b) Minimise the expression using Quine McCluskey method. 10
 $f(A B C D) = \sum m (1, 3, 7, 9, 10, 11, 13, 15)$
 (c) Realise expression using minimum NAND gates only. 4

$$y = A\bar{B} + A\bar{C} + C + AD + A\bar{B}C + ABC$$

4. (a) The circuit has four I/ps and two O/ps one of the outputs is to be true when the majority of inputs are false. The other o/p's is true only when there are equal number of true and false in the inputs. Design and implement combinational circuit using NAND gates only. 10
 (b) Implement an even parity checker for a 4 bit data, using 8 : 1 mux and inverters. 10

5. (a) Explain Master slave JK-FF. 10
 (b) Convert T FF to D FF. 10

6. (a) Design ripple counter for state diagram shown. 10

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            graph LR
            7((7)) --> 6((6))
            6 --> 5((5))
            5 --> 4((4))
            4 --> 3((3))
            3 --> 7
            
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- (b) Explain Johnson counter. 10

7. (a) What are decoding glitches and how these can be eliminated ? 10
 Explain universal shift register. 10
 (b) Implement 8-bit adder using 4-bit full adder. 10